1   1.   A method comprising:

2   providing a register accessible by a plurality of

3 processors; and

4   indicating whether data in said register is

5 available for a given processor.

1   2.   The method of claim 1 including indicating for

2 each of a plurality of processors whether the data is

3 available for a given processor.

1   3.   The method of claim 2 including requiring a

2 processor to wait to execute an instruction until the data

3 it needs to execute the instruction is available in one or

4 more registers.

1   4.   The method of claim 3 including providing a bit

2 for each item of data indicating whether a given processor

3 can access that data.

1   5.   The method of claim 4 including resetting said

2 bit when said data is accessed by a given processor.

1   6.   The method of claim 5 including providing a

2 register with a bit for each of a plurality processors,

3 enabling a processor to reset said bit when the data is no

4 longer useful to the processor, and preventing any

5 processor from writing data to said register until all of

6   the bits indicate that the data is no longer useful to any

7   other processor.

1   7.   The method of claim 6 including indicating the

2   processor which will utilize the data written into the

3   register.

1   8.   The method of claim 1 includes enabling a

2   plurality of processors to access a register at the same

3   time.

1   9.   The method of claim 1 including providing

2   specialized processors for mathematical operations and for

3   memory.

1   10.   The method of claim 1 including providing an

2   input processor, an output processor and coupling said

3   input, output and specialized processors to said register

4   through a cross-bar connection.

1   11.   An article comprising a medium storing

2   instructions that enable a processor-based system to:

3   make a register accessible by a plurality of

4   processing elements in said system; and

5   indicate whether data in said register is

6   available for a given processing element.

1　　　12. The article of claim 11 further storing
2　instructions that enable the processor-based system to
3　determine whether data is available in a register for a
4　particular processing element.

1　　　13. The article of claim 12 further storing
2　instructions that enable the processor-based system to
3　prevent execution of an instruction until the data needed
4　to execute the instruction is available in one or more
5　registers.

1　　　14. The article of claim 13 further storing
2　instructions that enable the processor-based system to
3　check a bit in said register for each item of data
4　indicating whether a processing element can access said
5　data.

1　　　15. The article of claim 14 further storing
2　instructions that enable the processor-based system to
3　reset said bit when said data is accessed by a processing
4　element.

1　　　16. The article of claim 15 further storing
2　instructions that enable the processor-based system to
3　identify in said register a bit for a processing element
4　from among bits for a plurality of processing elements,
5　reset said bit when the data is no longer useful to a
6　processing element, and to avoid writing said data to said

7 register until all the bits indicate that the data is no

8 longer useful to any other processing element.

1   17.   The article of claim 16 further storing

2 instructions that enable the processor-based system to

3 indicate which processing element will utilize the data

4 written into the register by another processing element.

1   18.   A digital signal processor including:

2   a plurality of processing elements; and

3   a register coupled to said plurality of

4 processing elements, said register including a plurality of

5 general purpose registers each accessible by said plurality

6 of processing elements, at least one of said registers

7 indicating whether data in said register is available for a

8 given one of said plurality of processing elements.

1   19.   The processor of claim 18 wherein said processing

2 elements are coupled to said register by a cross-bar

3 connection.

1   20.   The processor of claim 18 including a plurality

2 of registers each including a bit indicating for each of

3 said processing elements whether the data in the general

4 purpose register is available for a given processing

5 element.

1   21.   The processor of claim 18 wherein a processing
2   element must wait to execute an instruction until the data
3   it needs to execute the instruction is available in one or
4   more general purpose registers.

1   22.   The processor of claim 21 wherein each processing
2   element has a designated bit for each general purpose
3   register indicating whether a given processing element can
4   access the data.

1   23.   The processor of claim 18 wherein none of the
2   processing elements can write data to a general purpose
3   register until all of the bits indicate that the data is no
4   longer useful to any other processing element.

1   24.   The processor of claim 18 including a plurality
2   of general purpose registers, each of said general purpose
3   registers including a data section and a storage area for a
4   bit for each of said plurality of processing elements.

1   25.   The processor of claim 18 wherein said general
2   purpose register is accessible by each of said processing
3   elements at the same time.

1   26.   The processor of claim 18 wherein at least one of
2   said processing elements is an input processing element and
3   another of said processing element an output processing
4   element.

1   27.   The processor of claim 26 further including at
2   least one multiply and accumulate processing element.

1   28.   The processor of claim 27 including at least one
2   processing element for storing data in a random access
3   memory.

1   29.   The processor of claim 18 wherein no master
2   processing element is included and instead, the sequence of
3   operations in said digital signal processor is driven by
4   the availability in a general purpose register of data
5   needed to execute instructions.

1   30.   The processor of claim 18 including a plurality
2   of special purpose processing elements that may each access
3   a register at the same time.